

**Addendum No. 4 to RFP No. 0011204**  
**February 21st, 2004**

*Except as specifically modified herein, this RFP remains unchanged. Proposers are reminded that receipt of this Addendum No.4 must be acknowledged on Attachment A-1 or A-5 to the solicitation.*

Question 1:

In Section 5.1 - "Proof of concept" for each of the different Exhibit 3's regarding Phase 1 development, it says: "A unit/subassembly/Element produced for a Phase 1 development has/consists of microelectronics and Elements containing the same device rules, processing and speed as a device/subassembly/Element proposed for Phase 2, but not necessarily the same capacity or packaging"

Our question concerns the shrinkage of semiconductor technology which can make a major difference in device density/capacity, which changes every year or so - well within the 19 month period of the Phase 1 development. This question is for further clarification of the words "same device rules, processing and speed" which could be interpreted to relate to device functional/performance specifications, especially since it indicates at the end of the sentence that capacity does not necessarily have to be the same.

Does Section 5.1 of Exhibit 3's prohibit the development of a proof of concept device in Phase 1 with (for example 0.35-micron) technology that will later be built as a device for Phase 2, using a more dense technology (for example 0.18-micron), but where such a Phase 2 device will incorporate substantially the same design as the Phase 1 device?

Response 1:

Changing device layout rules and feature sizes has known impact on the radiation tolerance, susceptibility, and operability of microelectronic devices. As feature sizes shrink from one generation to the next, some of these aspects get better and some get worse.

The restriction on maintaining feature size from proto-chip to near-final product is considered valid in that it would permit the validation of a final design based upon a known "prototype" product and therefore would avoid conjecture. (As in "we can see that we have an upset rate of X and therefore if we do a feature shrink we *should* see an upset rate of Y.")

Question 2:

How rigid are the form factor requirements for the LM? I am talking about Figure 3 (page 20, JPL D-27605: High Speed LM Functional Requirements).

If a memory will meet the performance requirements of Phase 1 but probably not meet the form factor requirements in Phase 3 does it makes sense to propose for the LM especially if the mass of the packaged chip can not exceed 8 grams.

Response 2:

Item 10.1.1 of the functional specs for LM, the package described in Figure 3 and Table 4 is a recommended design (specs incorrectly say "shall") for the purpose of minimizing system impact if a new package size/style is proposed. Similarly, the inclusion of the word "shall" in 10.1.2 for 8 grams mass limitation is in correct and should be considered a recommendation as well.